REMARKS

The following is intended as a full and complete response to the Final Office Action dated April 8, 2009, having a shortened statutory period for response set to expire on July 8, 2009. The Examiner provisionally rejected claims 1-5, 7, 10-14, 16, 22-23, 25, 31-35 and 38-40 under the judicially created doctrine of obviousness-type double patenting. The Examiner rejected claims 1-4, 7, 10-17, 19-23, 25-27, 29-31, 34 and 38-40 under 35 U.S.C. § 103(a) as being unpatentable over Van Hook (U.S. Patent No. 6,342,892) in view of Bishop (SPARTA: Simulation of Physics on a Real-Time Architecture) and Dakhil (U.S. Patent No. 6,341,318).

Claim 1 is amended to include the limitations of claim 19 and, therefore, claim 19 is cancelled.

Rejections under Double Patenting

The Examiner provisionally rejected claims 1-5, 7, 10-14, 16, 22-23, 25, 31-35 and 38-40 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of co-pending Application No. 10/715,370 and claims 2, 8, and 19 of co-pending Application No. 10/715,440. Applicants acknowledge the double patenting rejection made in the Office Action and respectfully request that the rejection be held in abeyance until the pending claims are in condition for allowance. At such time, an appropriate terminal disclaimer will be filed, if still necessary.

Rejections under 35 U.S.C. §103(a)

Claim 1, as amended, recites the limitations of a DME control interface that is coupled to each of a PCE and a DME and comprises a first packet queue for receiving command packets from the PCE and transmitting the command packets to the DME, and a second packet queue receiving response packets from the DME and transmitting the response packets to the PCE. None of the cited references teaches or suggests these limitations.

Van Hook discloses a video game system having a central processing unit (CPU) and a coprocessor that produces audio and video signals, the coprocessor comprising a data movement controller and a signal processor. The CPU, via a CPU interface, reads from and writes to control registers within the signal processor to control the operation

of the signal processor (see Van Hook, column 17, lines 51-54). The signal processor executes audio and graphics tasks based on the register values stored in the registers within the CPU interface and transmits/receives data from memory via the data movement controller (see Van Hook, column 19, lines 41-45).

In the Office Action, the Examiner cites the signal processor as being equivalent to the claimed PCE, the data movement controller as being equivalent to the claimed DME and the control registers as being equivalent to the claimed DME interface. Applicants contend that the disclosed control registers cannot be equivalent to the claimed DME interface because, as clearly taught in Van Hook, the control registers are written to and read from only by the main processor and the signal processor (see Van Hook at column 19, lines 61-63). Importantly, none of the control registers receives data from the data controller, which the Examiner argues is equivalent to the claimed DME, and transmits that data to the signal processor. By contrast, amended claim 1 expressly recites the limitations of the DME interface comprising a second packet queue receiving response packets from the DME and transmitting the response packets to the PCE.

Bishop discloses an application-specific integrated circuit that can accelerate physics modeling in conjunction with a CPU. The Examiner relies on Bishop only to demonstrate a Physics Processing Unit (PPU). Thus, Bishop fails to cure the deficiencies of Van Hook set forth above.

The remaining references, Intel, Dakhil, Shiell, and Telekinesys, fail to cure the deficiencies of Van Hook (and Bishop) set forth above.

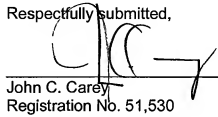
As the foregoing illustrates, no combination of the cited references teaches or suggests each and every limitation of amended claim 1. Therefore, these references cannot render obvious claim 1, or claims 2-5, 7, 10-17, 20-24 and 38, dependent thereon. For this reason, Applicants submit that claims 1 and claim 2-5, 7, 10-17, 20-24 and 38 are in condition for allowance.

Claims 25 and 31 recite limitations similar to those recited in claim 1 and are, therefore, allowable for at least the same reasons as allowable claim 1. The remaining claims depend from either allowable claim 25 or 31 and, therefore, are also in condition for allowance.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Final Office Action mailed September 9, 2009 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,



John C. Carey
Registration No. 51,530
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants